UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,891	09/25/2001	Daniel P. Drogichen	2070.006000/JAP P6802	9230

7590 06/17/2004

B. Noel Kivlin
Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C.
P.O. BOX 398
Austin, TX 78767-0398

EXAMINER	
LOHN, JOSHUA A	

ART UNIT	PAPER NUMBER
2114	9

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/963,891	DROGICHEN ET AL.
	Examiner	Art Unit
	Joshua A Lohn	2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-21,23-27,29 and 32-35* is/are rejected.

7)☒ Claim(s) *11,22,28,30 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2 and 4 recite the limitation "the failure" in line 1 of each claim. There is insufficient antecedent basis for this limitation in the claim. For the purpose of examination the examiner interprets the failure to be the predetermined condition mentioned in claim 1.

Claim 27 recites the limitation "the centerplane" in line 1. There is insufficient antecedent basis for this limitation in the claim. For the purpose of examination the examiner interprets the system to further include a centerplane.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-6, 8, 10, 12-16, and 23 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8, 11, 12, 15, 16, 17, and 22 of copending Application No. 09/963,890, as originally filed, in view of Suzuki et

al., United States Patent Application Publication 2001/0056553 A1, filed June 21, 2001, hereinafter referenced as Suzuki. This is a provisional obviousness-type double patenting rejection.

As per claim 1 of instant application, claim 1 of the copending application discloses detecting a predetermined condition triggering a reconfiguration of the computing system and reconfiguring a signal path affected by the condition form a first mode to a second mode responsive to detecting the condition. Claim 1 of the copending application fails to disclose leaving the unaffected system domains configured in the first mode and operating the affected system domains in the second mode and the unaffected system domains in the first mode.

Suzuki discloses leaving the unaffected system domains configured in the first mode (see paragraph 16, where only faulty paths are altered) and operating the affected system domains in the second mode and the unaffected system domains in the first mode (see paragraph 15, where failed paths are changed to a second mode and unaffected paths remain unaltered, or in a first mode).

It would have been obvious to one skilled in the art at the time of the invention to combine the invention of Suzuki with the limitations disclosed in claim 1 of the copending application.

This would have been obvious because, while the limitations of claim 1 of the copending application illustrate how a signal path, which is affected by a condition, is reconfigured, the copending application stops short of describing what happens to unaffected signal paths and what happens after the reconfiguration. Suzuki teaches of leaving an unaffected signal path domain in the first mode and operating it in that mode. It would have been obvious to do this to

allow for successful operation of domains that are not affected by the triggering condition. It would also have been obvious to operate the affected system domains in the second mode, as taught by Suzuki, because the reconfiguration is implemented to allow for this operation to occur.

As per claim 2 of the instant application, claim 2 of the copending application discloses detecting the predetermined condition includes detecting a failure. Since the system is a system of interconnects, it is inherent that a failure would have included an interconnect failure.

As per claim 3 of the instant application, claim 3 of the copending application discloses the computing system includes at least one system control board and wherein detecting the failure includes detecting the failure from the system control board.

As per claim 4 of the instant application, claim 4 of the copending application discloses detecting the predetermined condition from one of the system domains, which include the affected system domain.

As per claim 5 of the instant application, claim 5 of the copending application discloses including at least one system control board and the method further comprises notifying the system control board of the error from the affected system domain.

As per claim 6 of the instant application, claim 6 of the copending application discloses detecting the failure during normal operation, which is the same as first mode operation.

As per claim 8 of the instant application, claim 7 of the copending application discloses configuring an I/O switch, which is a first switch, defining a first end of the affected signal path from the first mode to the second mode. The switch is inherently in the affected domain because

it is part of the signal path being reconfigured and all domains in that path are affected. Claim 7 of the copending application further discloses configuring a crossbar switch defining a second end of the affected signal path from the first mode to the second mode.

As per claim 10 of the instant application, claims 11 and 12 of the copending application disclose operation in the first mode includes separating a plurality of information into two messages and transmitting the two messages in parallel, each on a respective half of the signal paths and operation in the second mode includes transmitting the two messages in series on a single half of the affected signal path. It is obvious from the rejection of claim 1 of the instant application, detailed above, that the unaffected system domains are in the first mode and the affected system domains are in the second mode.

As per claim 12 of the instant application, claim 8 of the copending application discloses the defining of the system domains.

As per claim 13 of the instant application, claim 15 of the copending application discloses dynamically reconfiguring the affected signal path includes dynamically reconfiguring the affected signal path from a normal mode into a degraded mode.

As per claim 14 of the instant application, claim 16 of the copending application discloses dynamically reconfiguring the affected signal path includes dynamically reconfiguring the affected signal path from a degraded mode into a normal mode.

As per claim 15 of instant application, claim 1 of the copending application discloses detecting a condition triggering a reconfiguration of the computing system and reconfiguring a

signal path affected by the condition form a first mode to a second mode responsive to detecting the condition. Claim 1 of the copending application fails to disclose operating the affected system domains in the second mode and the unaffected system domains in the first mode.

Suzuki discloses leaving the unaffected system domains configured in the first mode (see paragraph 16, where only faulty paths are altered) and operating the affected system domains in the second mode and the unaffected system domains in the first mode (see paragraph 15, where failed paths are changed to a second mode and unaffected paths remain unaltered, or in a first mode).

It would have been obvious to one skilled in the art at the time of the invention to combine the invention of Suzuki with the limitations disclosed in claim 1 of the copending application.

This would have been obvious because, while the limitations of claim 1 of the copending application illustrate how a signal path, which is affected by a condition, is reconfigured, the copending application stops short of describing what happens to unaffected signal paths and what happens after the reconfiguration. Suzuki teaches of operating an unaffected signal path domain in the first mode. It would have been obvious to do this to allow for successful operation of domains that are not affected by the triggering condition. It would also have been obvious to operate the affected system domains in the second mode, as taught by Suzuki, because the reconfiguration is implemented to allow for this operation to occur.

As per claim 16 of instant application, claim 1 of the copending application discloses detecting a condition triggering a reconfiguration of the computing system and reconfiguring a signal path affected by the condition form a first mode to a second mode responsive to detecting

the condition. Claim 1 of the copending application fails to disclose operating the affected system domains in the second mode and the unaffected system domains in the first mode.

Suzuki discloses leaving the unaffected system domains configured in the first mode (see paragraph 16, where only faulty paths are altered) and operating the affected system domains in the second mode and the unaffected system domains in the first mode (see paragraph 15, where failed paths are changed to a second mode and unaffected paths remain unaltered, or in a first mode).

It would have been obvious to one skilled in the art at the time of the invention to combine the invention of Suzuki with the limitations disclosed in claim 1 of the copending application.

This would have been obvious because, while the limitations of claim 1 of the copending application illustrate how a signal path, which is affected by a condition, is reconfigured, the copending application stops short of describing what happens to unaffected signal paths and what happens after the reconfiguration. Suzuki teaches of operating an unaffected signal path domain in the first mode. It would have been obvious to do this to allow for successful operation of domains that are not affected by the triggering condition. It would also have been obvious to operate the affected system domains in the second mode, as taught by Suzuki, because the reconfiguration is implemented to allow for this operation to occur.

As per claim 23 of the instant application, claims 17 and 22 of the copending application disclose a plurality of system domains, a plurality of signal paths, which are among the system domains because the system domains include signal paths, and a system controller capable of

detecting a condition triggering a reconfiguration and dynamically reconfiguring at least one signal path affected by the condition from a first mode to a second mode.

Claim Objections

Claim 11 is objected to because of the following informalities: in line 5 it states "the affected system domains in the first mode", however it is obvious from the other limitations and claims that this should state "the affected system domains in the second mode", and this is how it will be interpreted for the purpose of examination. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-9, 12, 13, 15-18, 21, 23, 24, 27, 29, and 32-35 rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki et al., United States Patent Application Publication 2001/0056553 A1, filed June 21, 2001, hereinafter referenced as Suzuki.

As per claim 1, Suzuki discloses a method for reconfiguring a signal path in a computing system including a plurality of system domains (a domain is interpreted as being functionally equivalent to the path, from initiating node to the outgoing line, through the system of Suzuki).

Suzuki further discloses detecting a predetermined condition triggering a reconfiguration of the computing system (see paragraph 15, where the predetermined condition is a failure). Suzuki discloses reconfiguring a signal path affected by the condition from a first mode to a second mode responsive to detecting the condition (see paragraph 16, where the routing table reconfigures a signal path). Suzuki discloses leaving the unaffected system domains configured in the first mode (see paragraph 16, where only faulty paths are altered) and operating the affected system domains in the second mode and the unaffected system domains in the first mode (see paragraph 15, where failed paths are changed to a second mode and unaffected paths remain unaltered, or in a first mode)

As per claim 2, Suzuki discloses detecting the predetermined condition includes detecting an interconnect failure (see paragraph 15, which describes detecting a failure in the interconnected path).

As per claim 3, Suzuki discloses the computing system includes at least one system control board and wherein detecting the failure includes detecting the failure from the system control board (see paragraph 16, where processor acts as system control board to receive notification from fault monitor).

As per claim 4, Suzuki discloses detecting the failure includes detecting the failure from the affected system domain (see paragraph 15, where the fault monitor will notify of failures in an affected system domain).

As per claim 5, Suzuki discloses the computing system includes at least one system control board and the method further comprises notifying the system control board of the error

from the affected system domain (see paragraph 16, where the processor acts as system control board to receive notification from monitor of an affected system).

As per claim 6, Suzuki discloses detecting the failure includes detecting the failure during first operations (see paragraph 17, where the constant monitoring would include detecting failure during first operation).

As per claim 7, Suzuki discloses detecting the failure includes detecting the failure upon reset (see paragraph 17, where the constant monitoring would include detecting failure upon reset).

As per claim 8, Suzuki discloses configuring a first switch in a first affected domain defining a first end of the affected signal path from the first to the second mode and configuring a crossbar switch defining a second end for the affected signal path from the first mode to the second mode (see paragraph 17, where the corrected routing of the switch is functionally equivalent to configuring a first and second end. The first switch corresponding to the input of the self routing switch and the crossbar switch corresponding to the self routing switch, which is functionally equivalent to a crossbar switch of this claim).

As per claim 9, Suzuki discloses the computing system includes a system control board and configuring the affected system domains includes configuring the system domains from the system control board (see paragraph 16, where each processor acts as control board to configure the relevant affected system domain).

As per claim 12, Suzuki discloses defining the system domains (see paragraph 13, where routing table defines composition of system domains).

As per claim 13, Suzuki discloses dynamically reconfiguring a signal path affected by the condition from a first mode to a second mode includes dynamically reconfiguring the signal path affected condition from a normal mode to a degraded mode (see paragraph 16, where transferring on alternative path is degraded from transmitting on originally expected path, the path before failure).

As per claim 15, Suzuki discloses a method for reconfiguring a signal path in a computing system including a plurality of system domains consisting essentially of the following elements. Suzuki discloses detecting a condition triggering a reconfiguration of the computing system (see paragraph 15). Suzuki also discloses reconfiguring a signal path affected by the condition from a first mode to a second mode responsive to detecting the condition (see paragraph 16). Suzuki further discloses operating the affected system domains in the second mode and the unaffected system domains in the first mode (see paragraph 15, where failed paths are changed to a second mode and unaffected paths remain unaltered, or in a first mode).

As per claim 16, Suzuki discloses a method for reconfiguring a signal path in a computing system including a plurality of system domains comprising the following elements. Suzuki discloses detecting a condition triggering a reconfiguration of the computing system (see paragraph 15). Suzuki also discloses reconfiguring a signal path affected by the condition from a first mode to a second mode responsive to detecting the condition (see paragraph 16). Suzuki further discloses operating the affected system domains in the second mode and the unaffected

system domains in the first mode (see paragraph 15, where failed paths are changed to a second mode and unaffected paths remain unaltered, or in a first mode).

As per claim 17, Suzuki discloses a computing system including a centerplane interconnecting the system domains (see paragraph 11, where the centerplane corresponds functionally to the self routing switch and interfaces). Suzuki further discloses a system controller capable of detecting a condition triggering a reconfiguration and reconfiguring a signal path affected by the condition from a first mode to a second mode (see paragraph 16, where the processors act as system controller to change mode of operation in event of triggering condition, in this case a fault).

As per claim 18, Suzuki discloses the system domains are dynamically configured (see paragraph 16, where domains configured dynamically by changes to the routing table).

As per claim 21, Suzuki discloses the centerplane comprises a plurality of crossbar switches interconnecting the system domains (see paragraph 15, where interfaces are functionally equivalent to crossbar switches in their use in the distribution of cells).

As per claim 23, Suzuki discloses a computing system including a plurality of system domains (see paragraph 11, where a domain is interpreted as being functionally equivalent to the path through system, from initiating node to the outgoing line, the system described has several of these domains). Suzuki further discloses a plurality of signal paths among the system domains (see paragraph 11, where the switch and interfaces of figure 1 correspond to plurality of signal

paths). Suzuki further discloses a system controller capable of condition triggering a reconfiguration and dynamically reconfiguring a signal path affected by the condition from a first mode to a second mode (see paragraph 16, where the processor is the system controller that dynamically reconfigures signal path).

As per claim 24, Suzuki discloses the system domains are dynamically configured (see paragraph 16, where the domains are configured dynamically by changes to the routing table).

As per claim 27, Suzuki discloses the centerplane comprises a plurality of crossbar switches interconnecting the system domains (see paragraph 15, where the interfaces are functionally equivalent to crossbar switches in their use in the distribution of cells).

As per claim 29, Suzuki discloses the plurality of signal paths includes: a plurality of data signal paths; a plurality of address signal paths; and a plurality of response signal paths (see paragraphs 12 and 14, which disclose data and address information passed through the paths, and paragraph 16, which discloses paths for response signals, in the form of results from the fault monitor).

As per claim 32, Suzuki discloses each signal path terminates at a first end in a first one of the system domains, routes through a crossbar switch, and terminates at a second end in a second one of the system domains (see paragraph 16, where, in the event of failure, the destination changes so a path that began in one domain can be diverted by the routing table to terminate at a second system domain).

As per claim 33, Suzuki discloses the system domains and the signal paths are configurable by configuring the first end, the second end, and the crossbar switch (see paragraph 16, where the altering of the routing table configures the second end and the switch, and the initiation of the message configures the first end, all to define the system domain).

As per claim 34, Suzuki discloses a computing system including a system controller (see paragraph 16, where the processor acts as system controller). Suzuki further discloses a plurality of system domains (see paragraph 11, where a domain is interpreted as being functionally equivalent to the path through system, from initiating node to the outgoing line, the system described has several potential of these domains). Suzuki also discloses at least one crossbar switch interconnecting the system domains (see paragraph 15, where the interfaces are functionally equivalent to crossbar switches in their use in the distribution of cells). Suzuki further discloses a plurality of signal paths, each signal path terminating at a first end in a first one of the system domains, routing through the crossbar switch, and terminating at a second end in a second one of the system domains (see paragraph 16, where, in the event of failure, the destination changes so a path that began in one domain can be diverted by the routing table to terminate at a second system domain). Suzuki also discloses a console connection over which the system controller can, responsive to a condition triggering a reconfiguration, reconfigure a plurality of the system domains affected by the condition and the crossbar switch to operate the affected signal paths in a first mode while the signal paths domains unaffected by the failure operate in a second mode (see paragraph 16, where the routing table is the console connection used by processor in response to a trigger, or failure, to reconfigure the interaction of the system

domains to change faulty paths to a first mode and leave all unaffected paths the same, operating in a second mode).

As per claim 35, Suzuki discloses a computing system including a plurality of system boards from which a plurality of system domains can be defined (see paragraph 11, which shows the interface system boards that are used to define the many domains, paths through the system from an initiating node to the outgoing line, of the system). Suzuki further discloses a centerplane including at least one crossbar switch interconnecting the system domains to provide a plurality of signal paths among the system boards (see paragraphs 14 and 15, where the switch and the interfaces are functionally equivalent to the centerplane, the interface is functionally equivalent to a crossbar switch in its use in the distribution of cells among the system boards). Suzuki also discloses a system control board hosting a system controller capable of defining the system domains, configuring the system domains and the crossbar switch to operate the signal paths in a first mode, and, responsive to a condition triggering a reconfiguration, reconfiguring the affected system domains and the crossbar switch to operate the affected signal paths in a second mode while the unaffected signals paths operate in the first mode (see paragraph 16, where the processor is the system control board that defines the system domains through use of the routing tables, these tables configure the switch and interfaces to operate in a second mode when a fault condition triggers a reconfiguration, the tables also maintain all unaffected signal paths operating in the first, non-faulty mode when no faults are detected).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14, 19, 20, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki.

As per claim 14, Suzuki discloses reconfiguring a signal path affected by a fault condition from a second mode to a first mode, where the second mode is a normal mode and the first mode is a degraded mode (see paragraph 15, where the degraded mode is the alternate path, which differs from the original intended destination). Suzuki fails to disclose transferring back from this degraded mode to a normal mode when a condition is detected.

Official notice is taken that it is well known in the art to return operation from a degraded operating mode back into a normal operating when a condition of no fault is detected. A well-known, illustrative example of returning from a degraded operating mode back into a normal operating mode is the boot operation of a standard personal computer. This boot operation is in a degraded mode if it must bypass a faulty hard drive and boot from a disk, when a fault is no longer detected in the hard drive of the example system, the boot operation returns to the normal mode of loading from a hard drive. This simplistic example illustrates that one of ordinary skill in the art relating to computer systems would have been motivated to return to a normal operating mode when a degraded operating mode is no longer necessary. The concept of returning to a normal operating mode from a degraded mode is well known in the art and applies

to various aspects of computer systems, such as a network switching system, when there is an obvious benefit to be gained.

It would have been obvious to one skilled in the art to return the invention of Suzuki to a normal operating mode in the event that a fault is no longer detected in the original path.

This would have been obvious because it is well known in the computer arts that operation in normal mode is preferred to operation in degraded mode. Since the invention of Suzuki must change the destination address of incoming packets when operating in degraded mode as a result of a card fault (see paragraphs 13-16), it would be beneficial to return to a normal operating mode, in which the added step of changing the address is unnecessary. The invention of Suzuki would have obviously benefited by returning to normal operating mode from a degraded mode in the event of a fault no longer existing.

As per claim 19, Suzuki discloses incoming transmission lines connected to system node, which are interpreted to be a part of the system domain (see paragraph 11). Suzuki fails to disclose these nodes including a system board, an expansion board, and an I/O board.

Official notice is taken that a system node could be a standard personal computer connected to a network. Standard personal computers are well known in the art to include a system board, or processor, an expansion board, such as that commonly used for memory modules, and an I/O board, or motherboard with peripheral slots. It is also well known in the art to have a standard personal computers connected to switching networks, such as that described by Suzuki in paragraph 11, to provide the benefit of user access to the network.

It would have been obvious to have a system board, an expansion board, and an I/O board in the system node of Suzuki.

This would have been obvious because these aspects would be included in a standard personal computer system that would provide the added value of a node that allows user access to the network.

As per claim 20, Suzuki obviously discloses the system board, expansion board, and I/O board comprise a system board set, where the node represents the system board set.

As per claim 25, Suzuki discloses incoming transmission lines connected to system node, which are interpreted to be a part of the system domain (see paragraph 11). Suzuki fails to disclose these nodes including a system board, an expansion board, and an I/O board.

Official notice is taken that a system node could be a standard personal computer connected to a network. Standard personal computers are well known in the art to include a system board, or processor, an expansion board, such as that commonly used for memory modules, and an I/O board, or motherboard with peripheral slots. It is also well known in the art to have a standard personal computers connected to switching networks, such as that described by Suzuki in paragraph 11, to provide the benefit of user access to the network.

It would have been obvious to have a system board, an expansion board, and an I/O board in the system node of Suzuki.

This would have been obvious because these aspects would be included in a standard personal computer system that would provide the added value of a node that allows user access to the network.

As per claim 26, Suzuki obviously discloses the system board, expansion board, and I/O board comprise a system board set, where the node represents the system board set.

Allowable Subject Matter

Claims 22, 28, 30, and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, as well as overcoming the objection for minor informalities mentioned above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is provided on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua A Lohn whose telephone number is (703) 305-3188. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoleil can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAL

SCOTT BADERMAN
PRIMARY EXAMINER